DOI: 10.21122/2220-9506-2024-15-4-316-322

Control of Integrated Circuits Crystals' Surface Microrelief and Defects of Hetero- and Submicrostructures by the Atomic Force Microscopy Method

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Received 04.10.2024
Accepted for publication 20.11.2024

Abstract

The aim of the work was to study the structure and defects of a channel transistor with two types of conductivity (*p* and *n*), the submicrostructures based on nickel silicide films, and the seed layers based on AlN using atomic force microscopy (including conductive or electric force method, which allow one to study the electrical conductivity of the material surface). The influence of the manufacturing technology and local oxide formation on the relief and structure of the *p*- and *n*-type transistor was established. The local oxide is necessary for the electrical isolation of the transistors from each other. The surface roughness is higher on the surface and outside the *p*-channel transistor than on the *n*-channel transistor. When examining the AlN layers both in the topography mode and in the adhesion mode, defects in the form of pores were revealed, which are places of electrical breakdowns, which worsens the properties of the such heterostructures. With an increase in the temperature and time of nitriding, the defects of the AlN layers significantly decrease. The conductive areas on the surface of the nickel silicides after rapid thermal treatment at 300 and 400 °C using electric force microscopy were detected, which shows incomplete formation of nickel silicide during the treatment. Thus, the efficiency of the atomic force microscopy method using a specialized conductive technique as a method for monitoring microelectronic components was demonstrated.

Keywords: control, transistor, microstructures, roughness, conductivity

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Для цитирования:
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For citation:
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Контроль микрорельефа поверхности кристаллов интегральных схем, дефектности гетеро- и субмикроструктур методом атомно-силовой микроскопии

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Поступила 04.10.2024
Принята к печати 20.11.2024

Целью работы было исследование структуры и дефектности канального транзистора с двумя типами проводимости (*p* и *n*), субмикроструктур на основе плёнок силицидов никеля, зародышевых слоёв на основе AlN с использованием атомно-силовой микроскопии (в том числе и проводящей или электросиловой методики, которая позволяет исследовать электрическую проводимость поверхности исследуемого материала) проведены. Установлено влияние технологии изготовления и формирования локального окисла на рельеф и структуру транзистора *p*- и *n*-типа. Локальный окисел необходим для электрической изоляции транзисторов друг от друга. Шероховатость поверхности выше на поверхности и вне *p*-канального транзистора, чем на *n*-канальном транзисторе. При исследовании слоёв AlN как в режиме топографии, так и в режиме адгезии выявлены дефекты в виде пор, которые являются местами электрических пробоев, что ухудшает свойства таких гетероструктур. При росте температуры и времени азотирования дефектность слоёв AlN существенно снижается. С применением электросиловой микроскопии установлены проводящие участки на поверхности силицидов никеля после быстрой термической обработки при 300 и 400 °C, что показывает неполное образование силицида никеля в процессе обработки. Таким образом показана эффективность метода атомно-силовой микроскопии с применением специализированной проводящей методики как метода контроля компонентов микроэлектроники.

Ключевые слова: контроль, транзистор, микроструктуры, шероховатость, проводимость

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Introduction

In the last decade, the demand for microelectronics and sensor products for various applications has been growing rapidly. An integrated circuit (IC) is one of the most important elements of the large electronic systems. In case of deterioration in the quality of an IC, the entire operating order of one electronic device or electrical appliance is disrupted, which plays an important role in organizing the life of a modern person [1]. During the manufacture of ICs, their performance and stability are affected by various factors, including the size effects, microrelief, the presence of secondary etching reaction product residues on the walls of elements and on the bottom of the reliefs, the presence of local defects in dielectric and metallized films, the structure and phase composition of semiconductor structures, etc. [2]. The microrelief control is usually carried out using optical microscopy and/or scanning electron microscopy. However, with the reduction of design standards for the manufacture of microcircuits, this type of microscopy cannot be used due to the limited resolution of the methods, as well as the complexity of preparing samples for control [3].

Reducing the size affects the change in the properties of the MEMS elements [4]. For example, reducing the size of MOS transistors leads to deterioration of their characteristics [1]. To solve this problem, the transistor structure is changed by introducing new elements and materials. The use of silicides (for example, as transition layers) in the production of Schottky diodes, infrared sensors, gates on field-effect transistors, MEMS technology, metal compounds in microchips, the creation of microstructures on quantum wires and quantum dots has improved their characteristics [5, 6]. However, the ongoing miniaturization of ICs places many new demands on such materials. For example, NiSi film has low electrical resistance (10.5–18 μOhm cm at room temperature) and resistance to electromigration, but the main disadvantage is low thermal stability up to temperatures of 650 °C, which leads to the transition of the conductive phase of NiSi to $NiSi_2$ with a higher specific resistance. Improvement of the morphological and phase stability of silicides at elevated temperatures is achieved by doping with Pt, Pd or Rh elements [7, 8], as well as the rapid thermal treatment (RTT). The metallic nature of the conductivity, low electrical resistance, thermal and chemical stability, and low the Schottky barrier height on *p*-type silicon (0.28 eV) contribute to their successful application in microdevices [6]. In the thin films of the silicides used, the grain size and surface roughness are important parameters determining the level of their functional properties. There are no dependencies in the scientific literature linking the RTT temperature with the roughness, grain size and reverse current density of the Schottky diode.

Heterostructures based on aluminum nitride (AlN) are promising materials for power, high-frequency and optoelectronic devices. To grow AlN layers [3] with a smooth surface, the layer growth temperature is changed. However, this may cause defects in the structures.

The size effects [4] in the transition to micro- and nano-sizes of systems make the tasks of complex research of the properties of functional and structural materials in microelectronics relevant. Traditional research methods do not allow detecting phenomena that determine the properties of the material at the micro- and nanolevel. Therefore, there is a need to use modern high-resolution methods, which include atomic force microscopy and nanoindentation, which make it possible to study the structure, physical, mechanical, electrical and magnetic properties of materials and systems during development and operation.

The aim of the work was to study and control the structure and defects of a channel transistor with two types of the conductivity (*p* and *n*), submicrostructures based on the nickel films and a seed layer based on AlN using atomic force microscopy.

Materials and research methods

Several samples of the following type were used for the study:

– the channel transistor with two types of conductivity (*p* and *n*);

– the submicrostructures based on the nickel films after the rapid thermal treatment at 300 and 400 °C;

– the AlN based seed layers.

The channel transistor is manufactured using CMOS technology with one metallization level. Design standards are 5.0 μm. The substrate is of type KEF 4.5 (electronic silicon doped with phosphorus with a specific resistance of 4.5 Ohm cm). Then, a local oxide is formed on the surface for electrical insulation of the transistors from each other. The local oxide is created thermally in a dry oxygen

atmosphere at a temperature of 1000 °C. The total thickness of the formed oxide is 0.8 μm. In this case, 0.4 μm of substrate silicon is consumed.

The nickel films with a thickness of ≈40 nm [10, 11] were deposited on silicon substrates by magnetron sputtering of a nickel target with a purity of 99.5 %. After deposition, the nickel film on silicon was subjected to the rapid thermal treatment (RTT) in the heat balance mode using a JetFirst 100 setup (Jipelec Qualiflow Therm, Montpellier, France). The back side of the silicon substrates was irradiated with an incoherent light flux of the constant-power quartz halogen lamps in a nitrogen environment for 7 s. Heating was carried out until a temperature of 400 °C was reached.

The AlN germinal layers with a thickness of 85 nm were grown by the plasma molecular beam epitaxy (at the temperature of the Al_2O_3 substrate T = 780 °C) with the different nitriding times and temperatures:

– the nitriding time 90 min at $T_{(Al)}$ = 1235 °C;
– the nitriding time 90 min at $T_{(Al)}$ = 1237 °C;
– the nitriding time 120 min at $T_{(Al)}$ = 1237 °C.

For the visualize the morphology, control the microrelief and defects of the above samples, we used a Dimension FastScan atomic force microscope (Bruker, USA) in the PeakForce QNM mode (nanomechanical mapping) using a standard silicon cantilever of the CSG1-SS type (TipsNano, Russia) with a tip curvature radius of 5 nm and a cantilever stiffness of 0.3 N/m, as well as the C-AFM mode – electric force microscopy using a silicon cantilever of the SCM-PIT type (Bruker, USA) with a conductive PtIr coating, a tip curvature radius of 20 nm and a cantilever stiffness of 2.8 N/m.

Results and discussions

Based on the results of the study of two types of transistors (Figure 1), it was found that the surface structure of the *p*-channel transistor (Figure 1*b*) and the profile drawn across the transistor (Figure 1*d*) show the presence of a continuous oxide strip with a height of about 200–250 nm and a width of up to 0.8–1.0 μm at the transistor boundary. The studies were carried out both on the surface of the transistors and outside the surface of the transistors. The main internal structure of the *p*-channel transistor is developed and granular (Figure 1*f*), has almost the same height as the surface outside the transistor. The surface of the *n*-channel transistor (Figure 1*c*) has a uniform structure and height (about 300 nm) both along the length and width of the transistor (Figure 1*e*). The structure of the *n*-channel transistor is smoother compared to the *p*-channel (Figure 1*f*). The surface roughness (Table 1) is higher on the surface and outside the *p*-channel transistor than on the *n*-channel transistor.

The revealed relief and structure are due to the formation of local oxide during the production process.

Table 1

Surface roughness of transistors

Type of transistor	Research location	Roughness		
		Ra, nm	Rq, nm	Rz, nm
p-type	Inside	4.98	7.36	12.2
	Outside	12.1	14.7	11.8
n-type	Inside	4.08	5.46	16.3
	Outside	4.78	6.16	8.07

The morphology of AlN germinal layers at different nitriding times is almost the same – it consists of the smooth rounded structures with the uneven edges (Figure 2).

It should be noted that there are a large number of pores on the AlN germinal layer at a nitriding time of 90 min at $T_{(Al)}$ = 1235 °C (Figure 2*a*, shown by yellow arrows). In the adhesion mode, these areas have low adhesion (Figure 2*g*, dark areas are shown by blue arrows). With an increase in the nitriding time to 120 min at $T_{(Al)}$ = 1237 °C, the number of pores decreases significantly (Figure 2*b*, c) and the surface relief decreases (Figure 2*d*–*f*). Such pores are places of the electrical breakdowns, which worsens the properties of such heterostructures.

On the submicrostructures based on the nickel silicide after RTT at 300 and 400 °C, when studying by the atomic force microscopy with a conductive mode, it was possible to identify the conducting and non-conducting regions (Figure 3 and 4), i. e. Ni and NiSi, respectively. The conducting regions (light regions in Figures 3*b* and 4*b*, *d*, dark regions in Figure 3*c*).

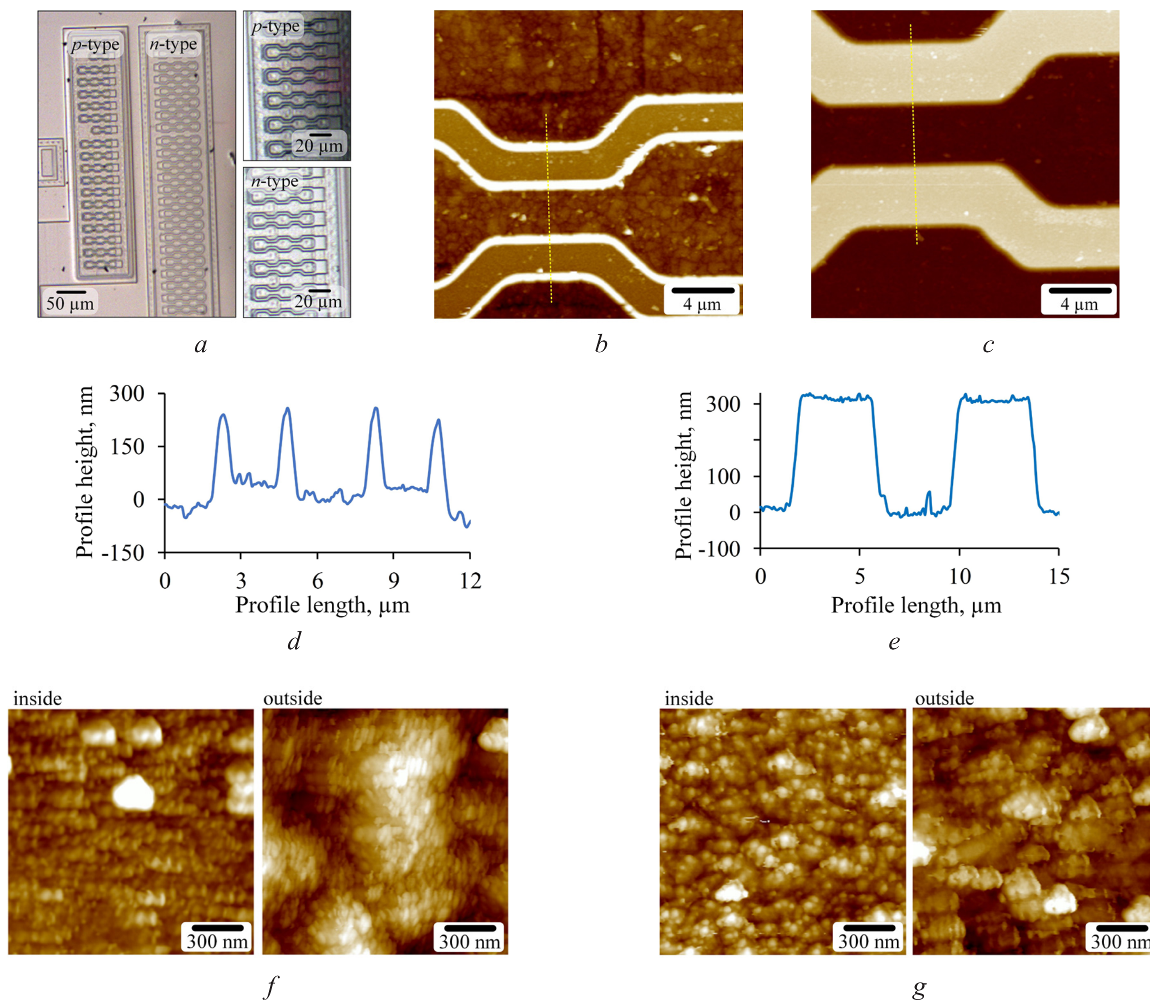
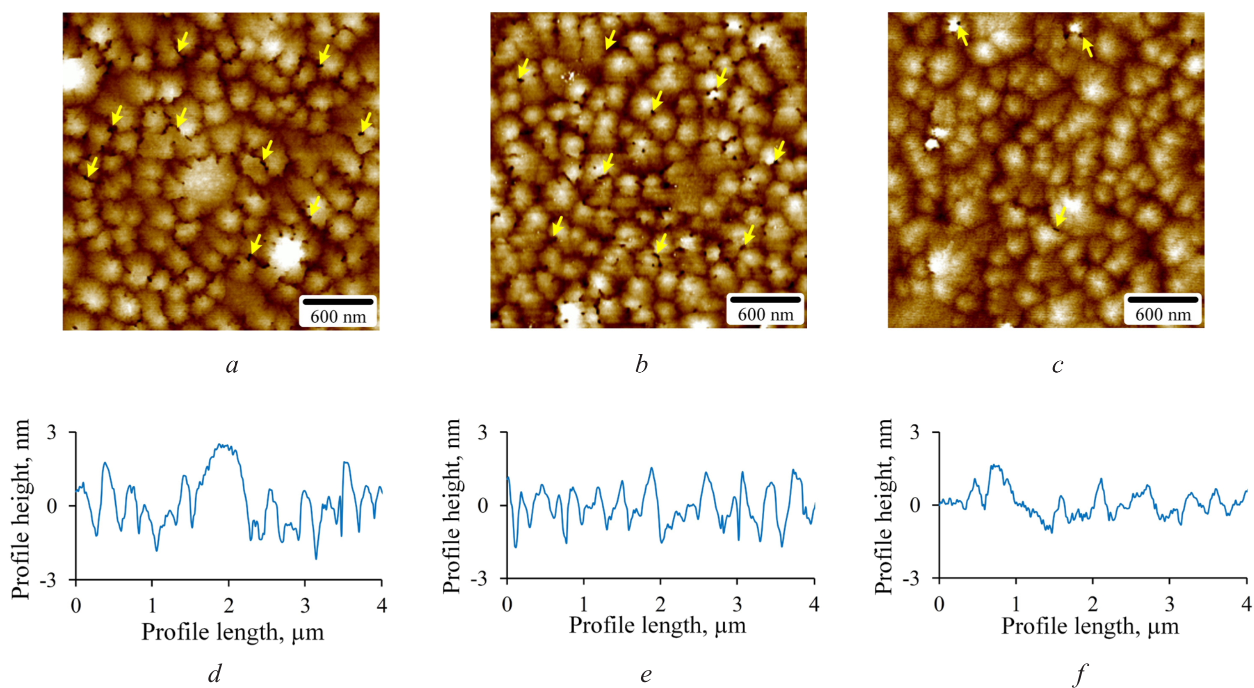


Figure 1 – Optical (*a*), AFM structure (*b*, *c*, *f*, *g*) and surface profiles (*d*, *e*) of *p*-type (*b*, *d*, *f*) and *n*-type (*c*, *e*, *g*) transistors



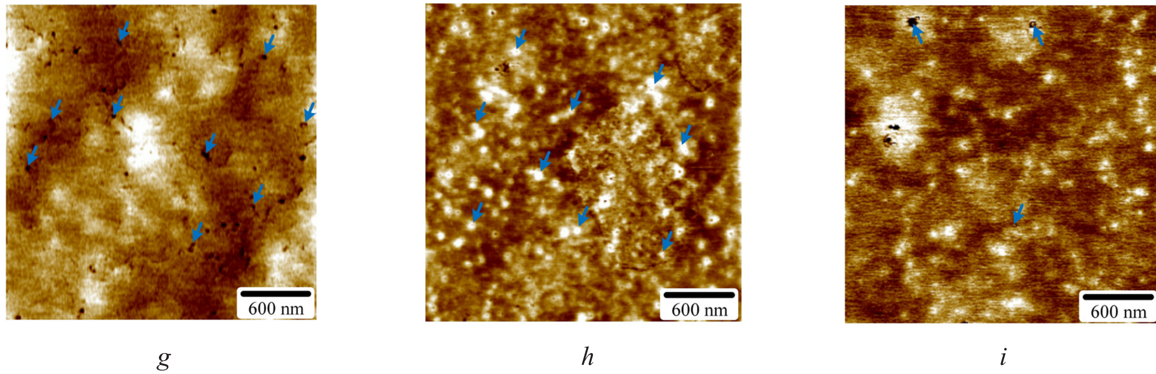


Figure 2 – AFM structure (topography (*a*–*c*) and adhesion (*g*–*i*) modes, fields 3×3 μm^2) and surface profiles (*d*–*f*) of samples with an 85 nm thick AlN germinal layer with different nitriding times: *a*, *d*, *g* – nitriding time 90 min at $T_{(Al)}$ = 1235 °C; *b*, *e*, *h* – nitriding time 90 min at $T_{(Al)}$ = 1237 °C; *c*, *f*, *i* – nitriding time 120 min at $T_{(Al)}$ = 1237 °C

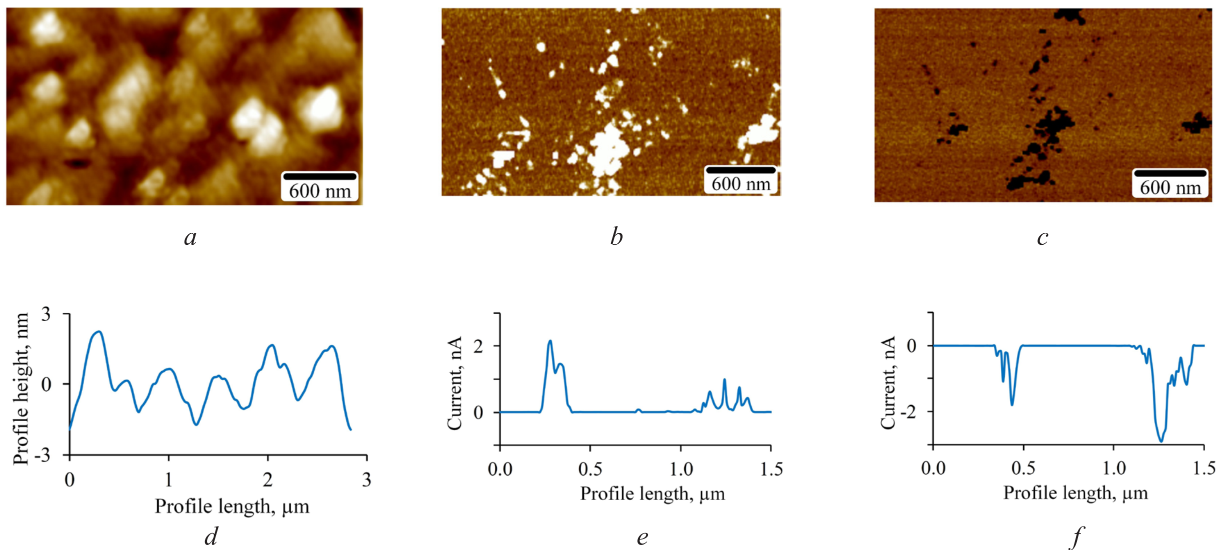


Figure 3 – AFM images of the nickel silicide-based submicrostructures after 400 °C with the conducting defects: *a* – topography; *b* – conducting mode at a voltage of +4 V; *c* – conducting mode at a voltage of -4 V

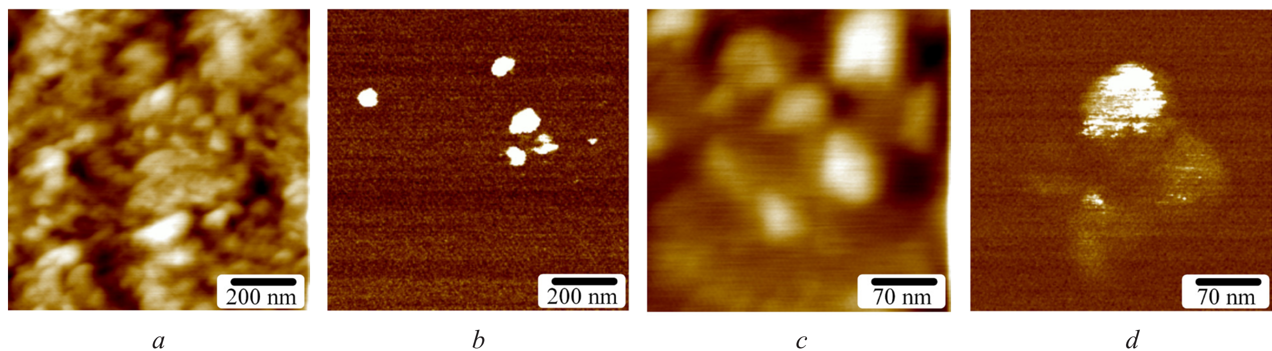


Figure 4 – AFM images of the nickel silicide-based submicrostructures after 300 °C with the conducting defects: *a*, *c* – topography; *b*, *d* – conducting mode at +4 V

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When a voltage of ±4 V is applied, the conductive regions have a current from -2 (when a negative voltage of -4 V is applied, dark areas in Figure 3*c*) to 2 nA (when a positive voltage of 4 V is applied, light areas in Figures 3*b* and 4*b*, *d*).

Conclusion

The influence of the manufacturing technology on the microstructure and surface properties of the microelectronic components was established. The research and defect control were carried out on a channel transistor with two types of the conductivity (*p* and *n*), submicrostructures based on the nickel films after rapid thermal treatment at 300 and 400 °C and seed layers based on AlN using the atomic force microscopy. Two scanning modes were used: the PeakForce QNM (nanomechanical mapping) and C-AFM (electrical force). The influence of the manufacturing technology and local oxide formation on the relief and structure of the *p*- and *n*-type transistor was established. Defects in the form of the pores were revealed during the study of AlN heterostructures both in the topography mode and in the adhesion mode. With increasing temperature and time of nitriding, the defectiveness is significantly reduced. The conductive areas on the nickel silicides were established after RTT of 300 and 400 °C using electric-force microscopy. Thus, the effectiveness of the atomic force microscopy method using specialized conductive techniques as a method for monitoring the microelectronic components is demonstrated.

Acknowledgments

This research was supported by the grant of Belarusian Republican Foundation for Fundamental Research BRFFR No. T23ME-010 and T17KIG-009.

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