

Parallel Processor for Pattern Recognition

Michail Tatur

e-mail: tatur@bsuir.by, tatur@i-proc.com

Belarusian State University of Informatics and Radioelectronics, Minsk, Belarus

“Intellectual Processors” Ltd., Minsk, Belarus

www.i-proc.com

Our neuron like parallel processor has been implemented as operating sample and it consists of hardware (HW) part on FPGA and Internal software (SW), Fig1. Internal SW provides configuration of FPGA and internal control unit for control and synchronization of hardware modules. Obviously, the various HW implementations will meet the unique Internal SW.

To test, verify and evaluate the developed technical solution of processor and to demonstrate it operating we have developed the special program tool: External SW for normal computer. External computer is used as control (Host) and neuron like processor is used as coprocessor. Computer`s interface is USB, but can be PCI, Ethernet etc.

External SW consists of three levels.

Low level SW provides:

- Data exchanging between Host-computer and Coprocessor;
- API-library for development of external program applications on higher levels;
- Program emulator, which simulates the implemented HW-coprocessor and provides to test and demonstrate External SW without real HW.

Middle level SW provides:

- Programming the initial modes and tunes of coprocessor, input of processing data and display of accepted numerical results;
- Programming of modes and criteria of decision making in post-processing phase.

High level SW (it is not shown in fig.1) conducts applied programs, for instance human portrait recognition, finger prints identification, image search in big data bases and etc. Note! In similar programs of high level the classification task realized by neuron like processor occupies a predefined part in common volume of algorithms. Obviously, the final advantage will be higher when classification task needs large computing charges (it will be in cases, when classification task operates with big number of informative features and huge number of classes).

Middle and Low level SW help us to create the new versions and prototypes of analogues processors with various apparatus platforms and with given technical requirements more quickly and cheaply.

Note. Accuracy (sensitivity, specificity) of classification does not depend on HW implementation of coprocessor and its computer architecture. It is complex property and depends on math model, learning data set, learning algorithm, choice of informative features and real pattern distribution in feature space. In case we are ready to research this problem in context of considered computer architecture and whole technical problem.

The present sample has been implemented with board Spartan 6 FPGA Evaluation Kit. In FPGA chip the 8 processors has been realized. Each processor element performs the original identification model and conducts the 16 digits of input/output data with fixed point. We can provide the structure scheme of processor element, if it is necessary, but I think it is not interesting for potential customer.

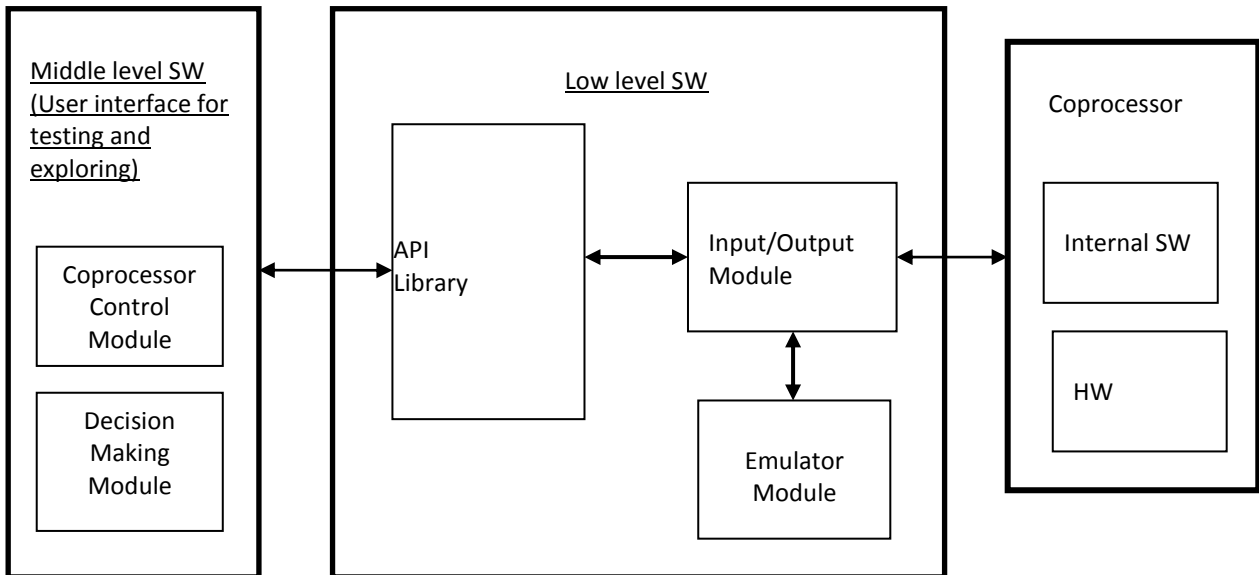


Fig.1 General scheme of evaluation system

For concrete HW solution the experimental assessments of calculation time for macro operation has been received. So, processing time of one informative feature is 50 nS. The total processing time of classification task can be calculated by expression

$$T \approx (50nk) / N_k$$

Where n – is number of informative features;

k – is number of classes;

N_k – is number of processing element in parallel processor.

We think the intellectual property and know-how are contained in technology of fast creating of HW+SW processor prototypes with defined technical requirements, limitations, with customer`s HW platform. Therefore we don`t interested in transfer our sample (SW or/and HW) in such form. To test and evaluate our technology we propose to carry out the analogues development under the specific Customer`s technical requirements. The customer might define:

- Number of informative features;
- Number of classes;
- Number of digits of input/output data;
- Computer performance (time of classification task processing);
- HW platform (DSP, FPGA, multicore CPU, GPU, cluster) with detail.

To test and evaluate the our math model Customer might give us:

- Learning data set;
- Expected efficiency (sensitivity/specificity) of classification;
- Perhaps, achieved efficiency (sensitivity/specificity) of classification with same learning data set on alternative math model (ANN, SVM and etc.) for comparison.

Then we are ready to provide fast researching with use own tools and present results to Customer without or with know-how and intellectual property transfer and take part in implementation work of our technical solutions in completed system of Customer. Furthermore, we have ideas to develop our model and computer architecture in direction of functionality enhancing. It can be subject for collaboration too.